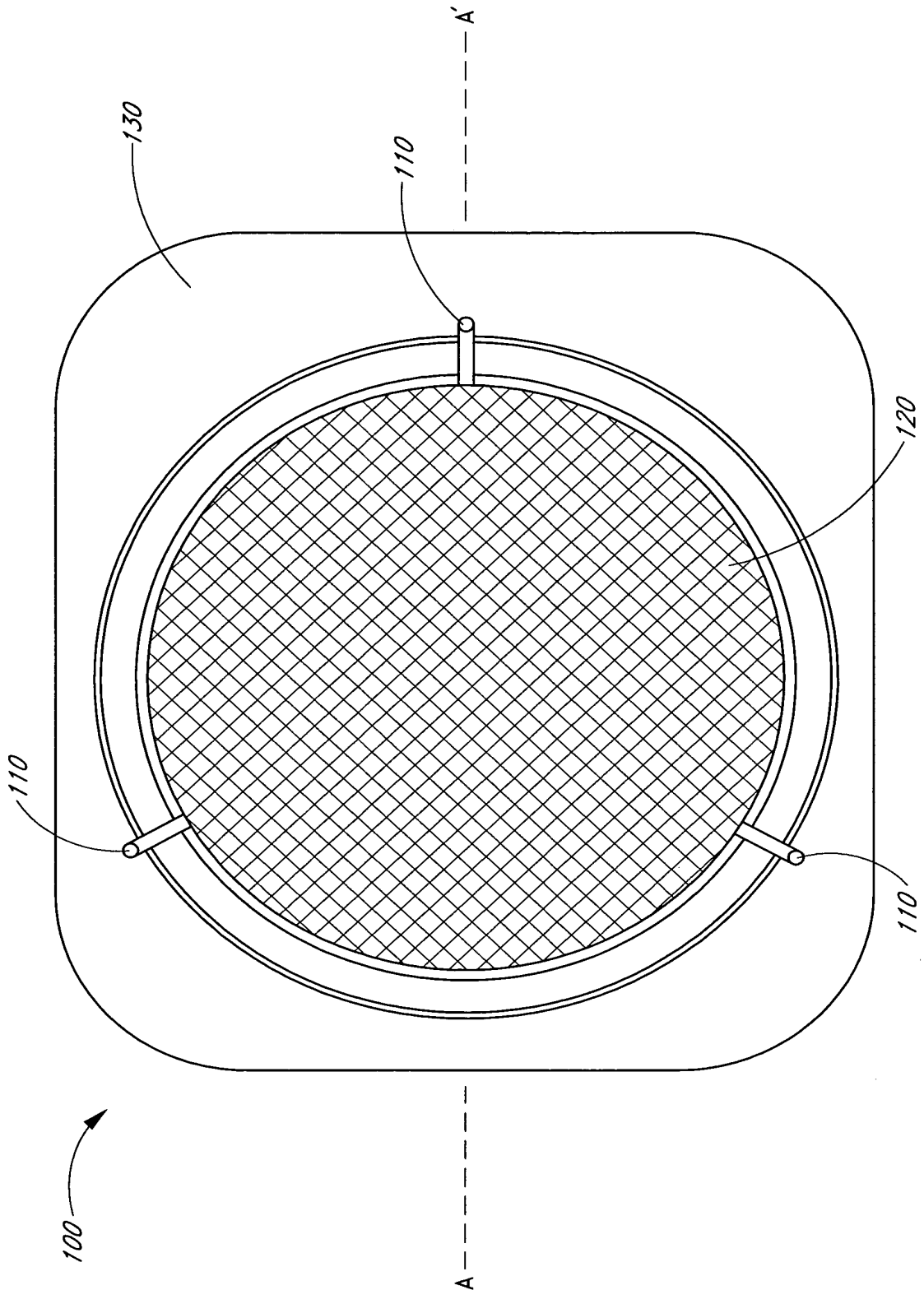


## TWO-STAGE LOAD FOR PROCESSING BOTH SIDES OF A WAFER

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**FIG. 1A**

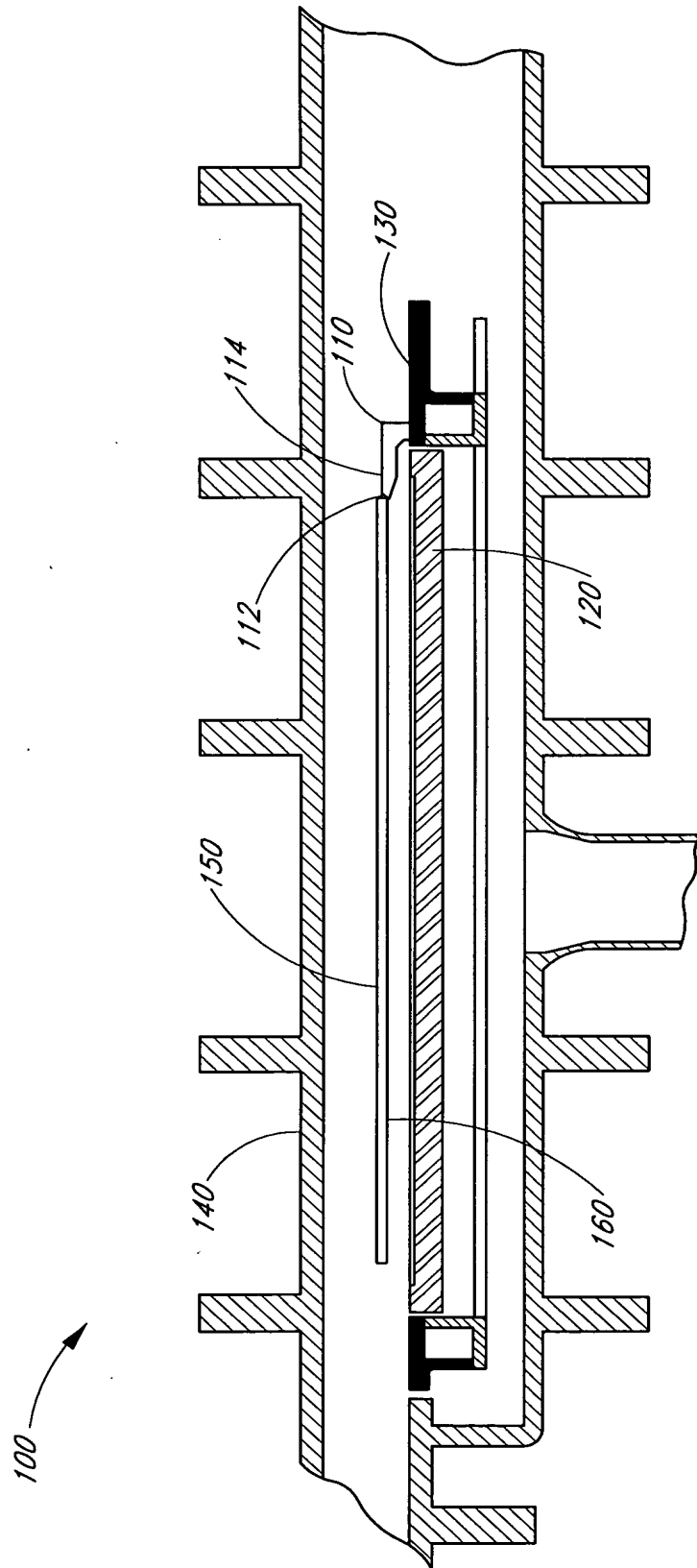
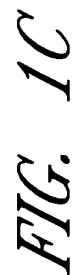


FIG. 1B

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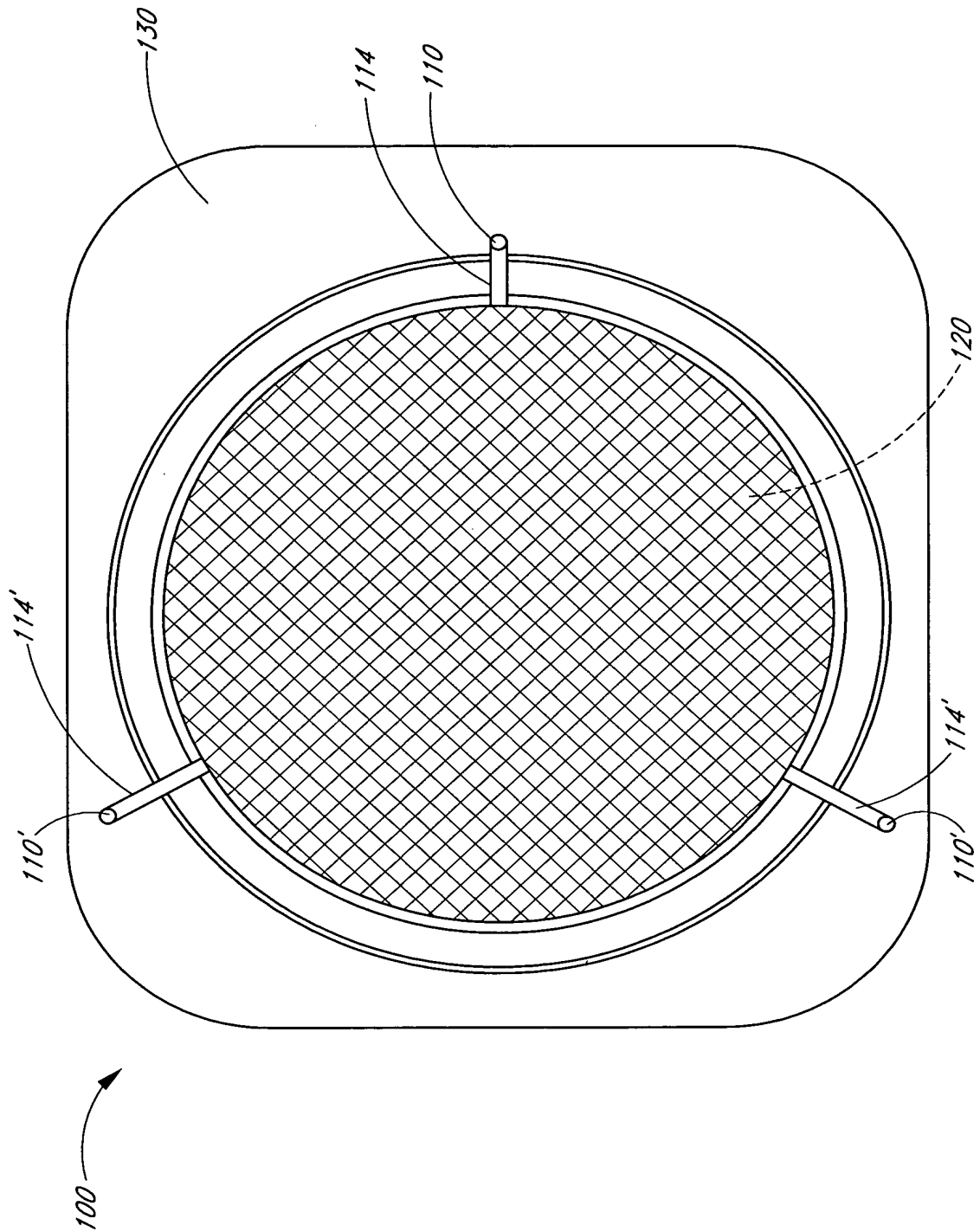


**TWO-STAGE LOAD FOR PROCESSING BOTH SIDES OF A WAFER**

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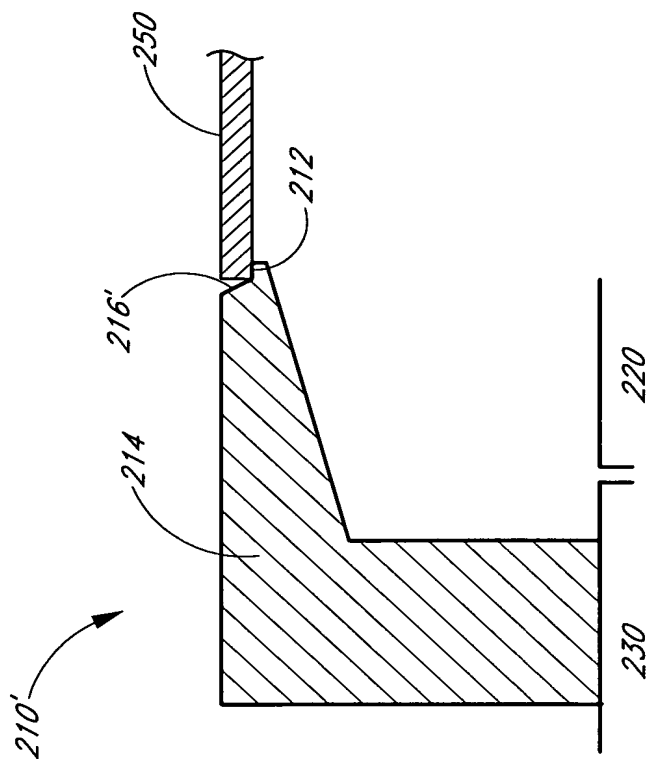


FIG. 2B

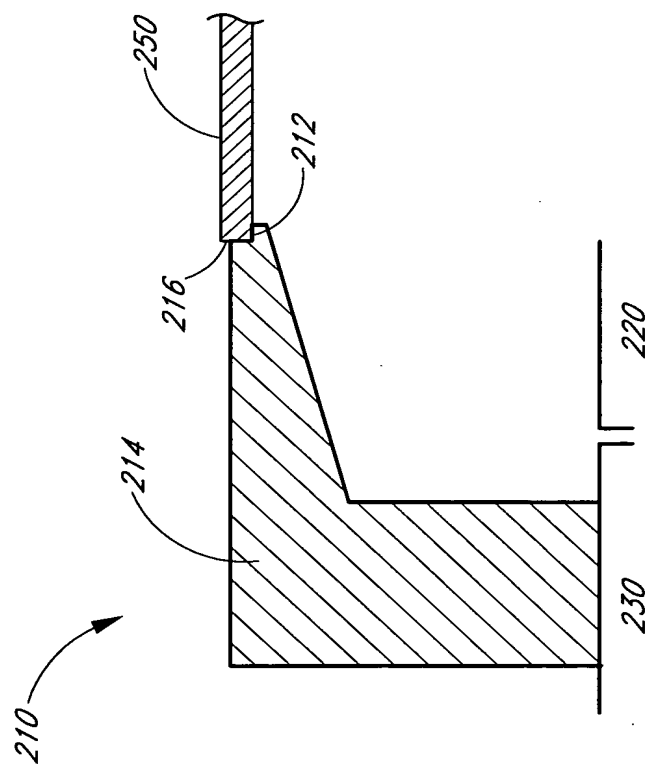


FIG. 2A

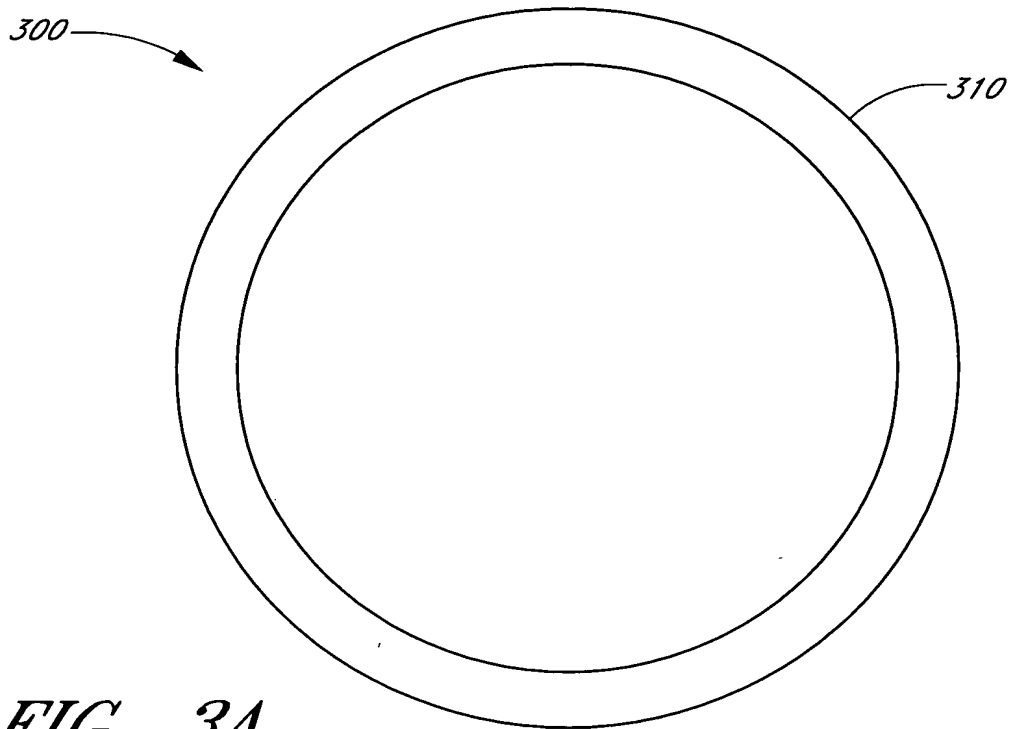


FIG. 3A

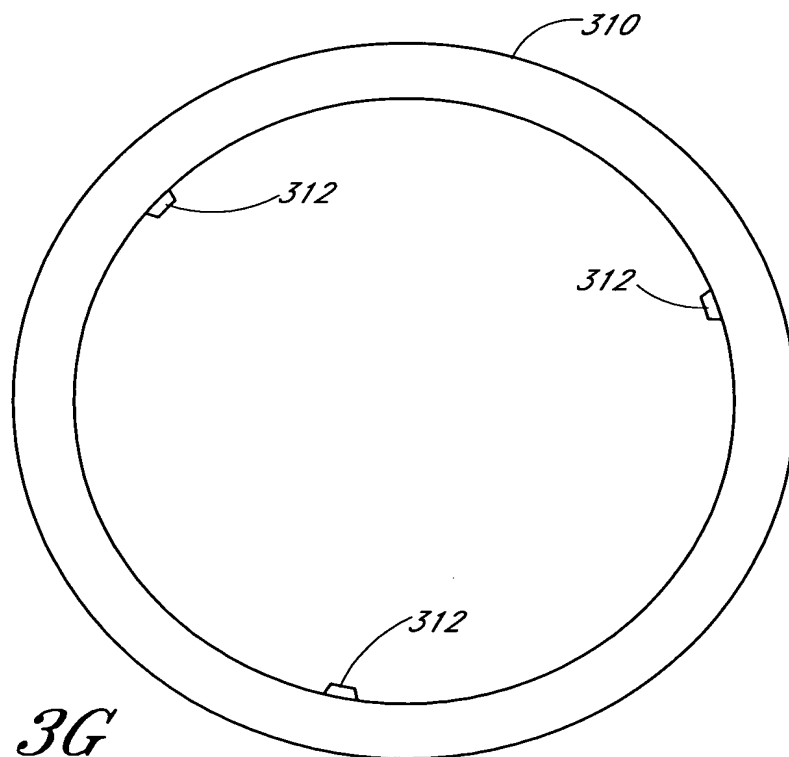


FIG. 3G

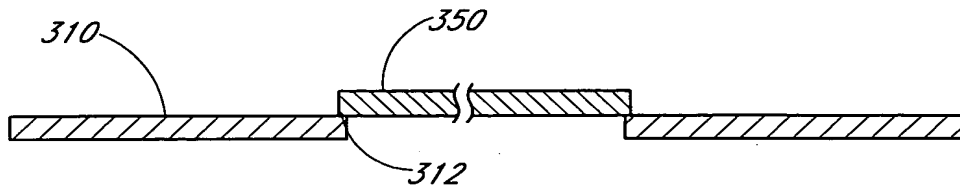


FIG. 3B

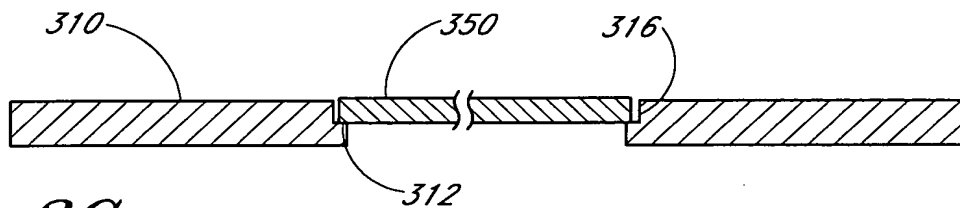


FIG. 3C

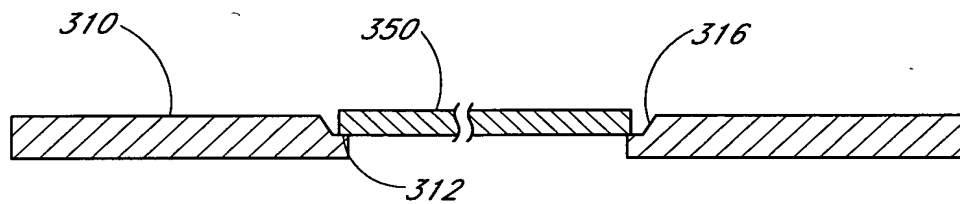


FIG. 3D

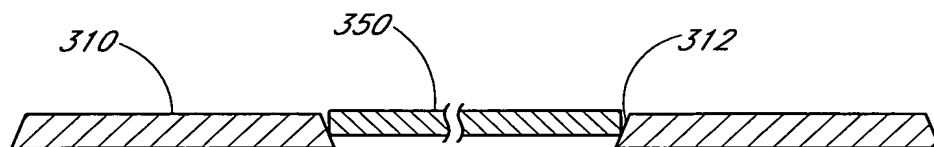


FIG. 3E

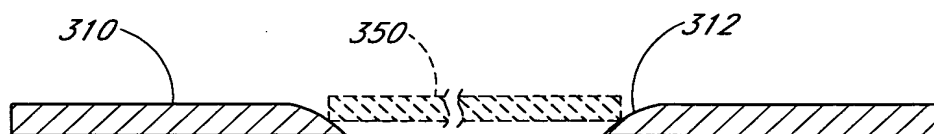


FIG. 3F

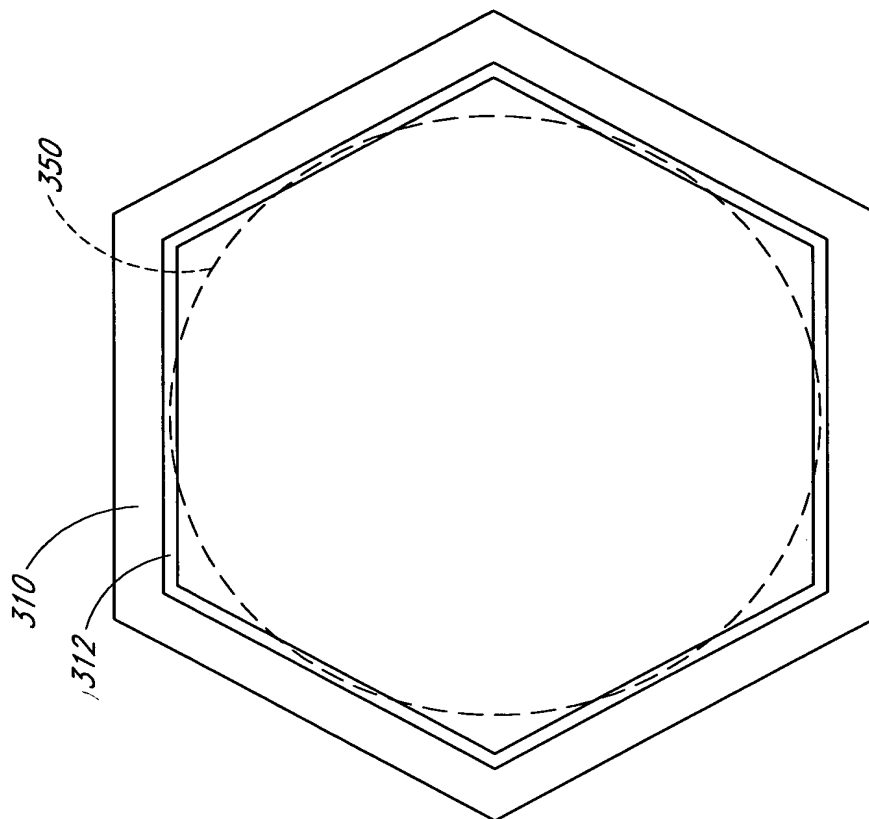


FIG. 3I

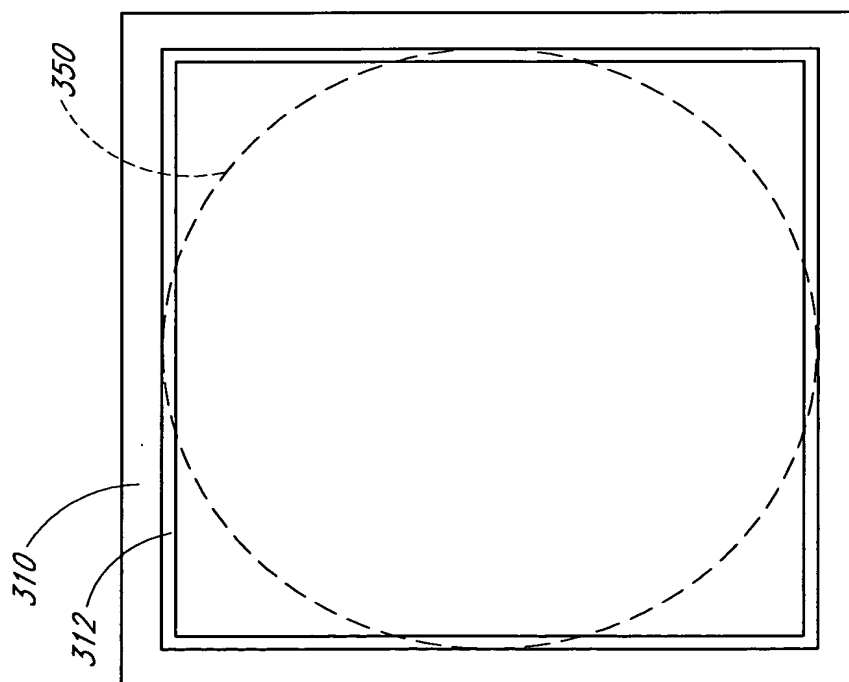


FIG. 3H

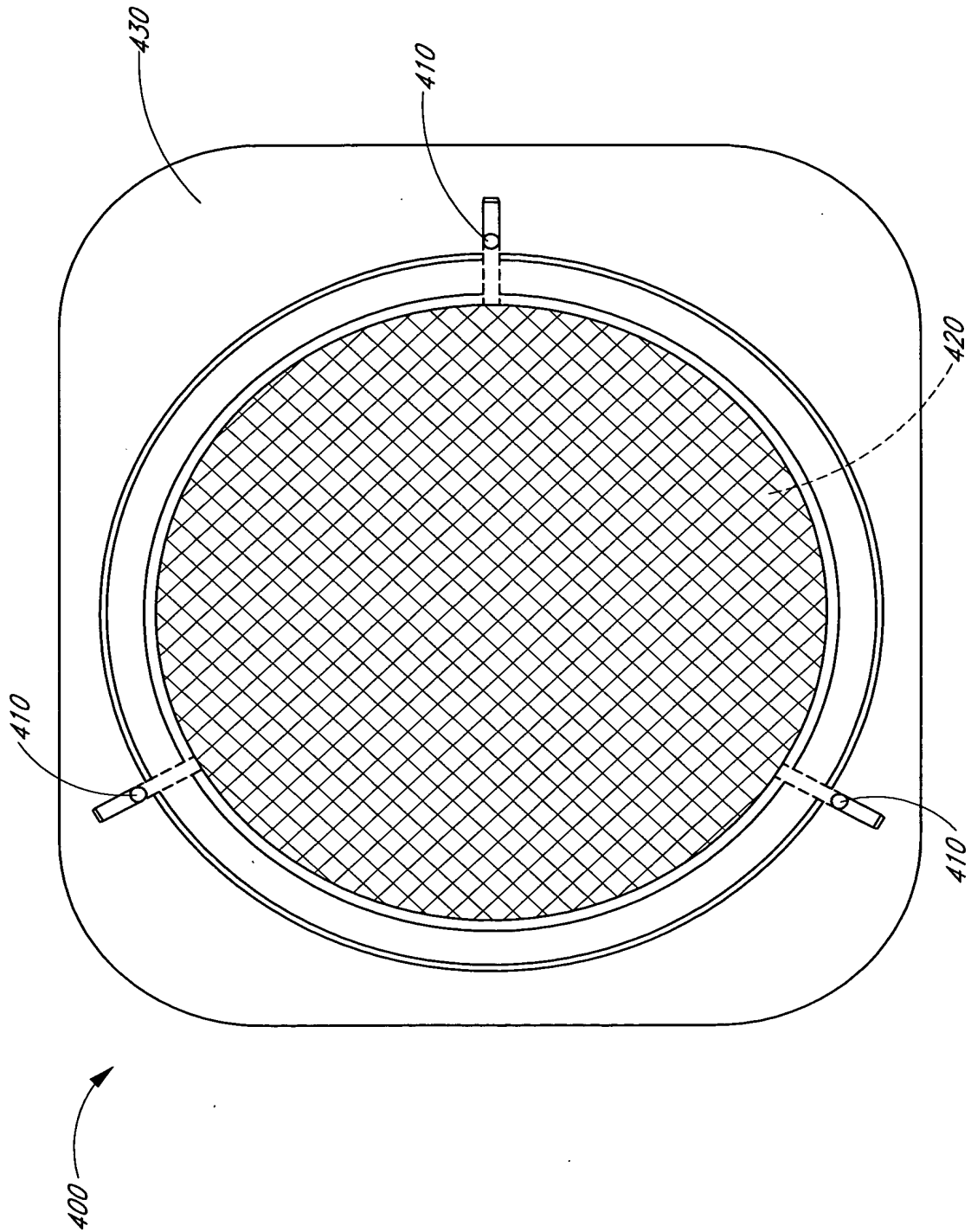


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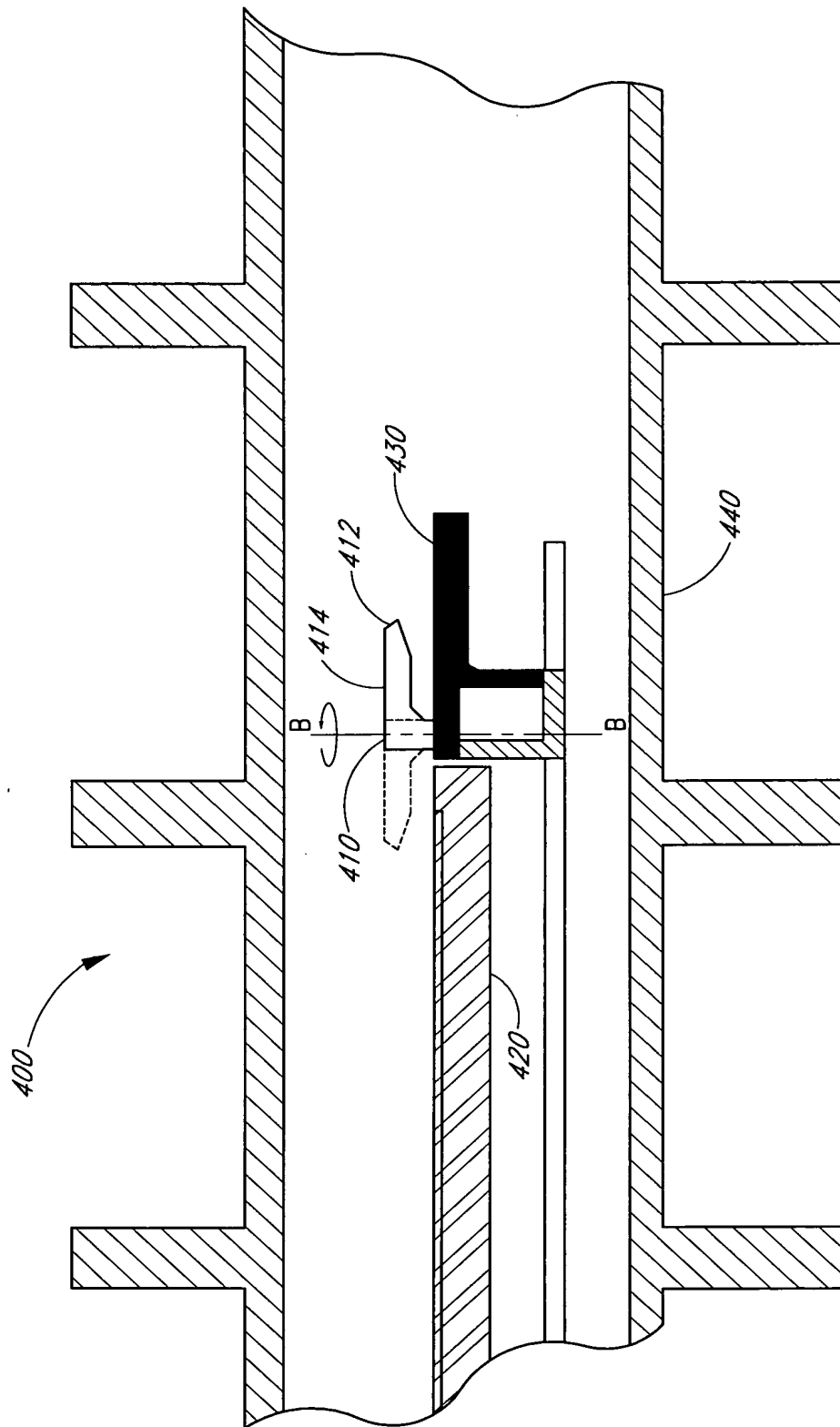


FIG. 4B

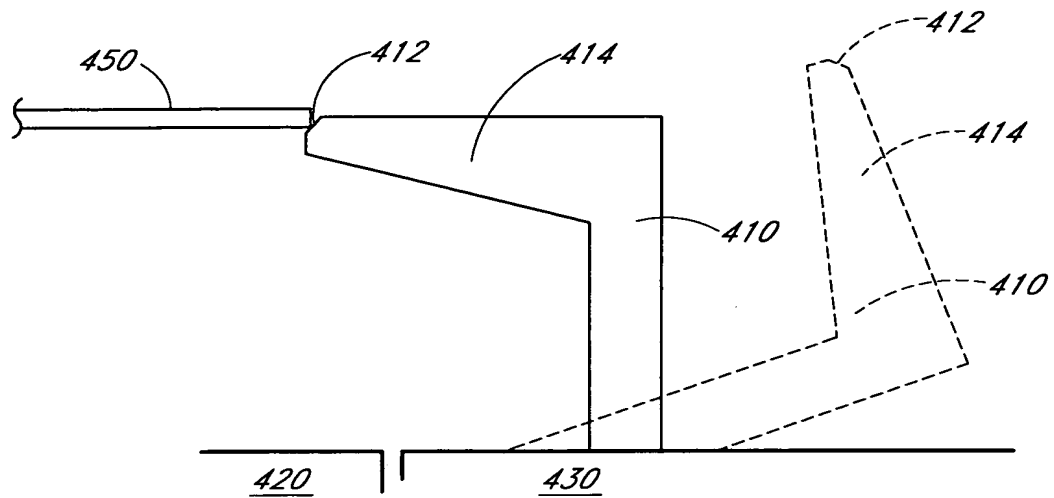


FIG. 4C

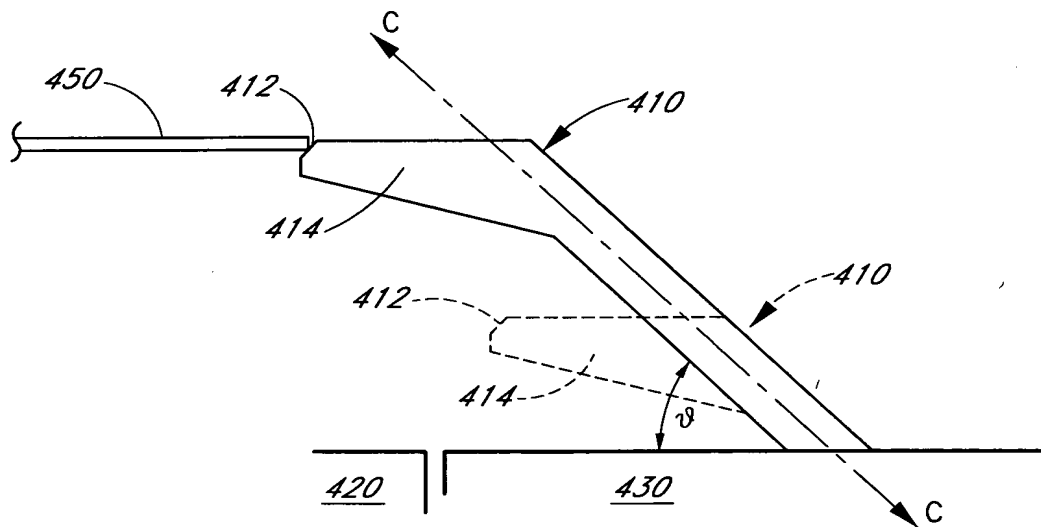


FIG. 4D

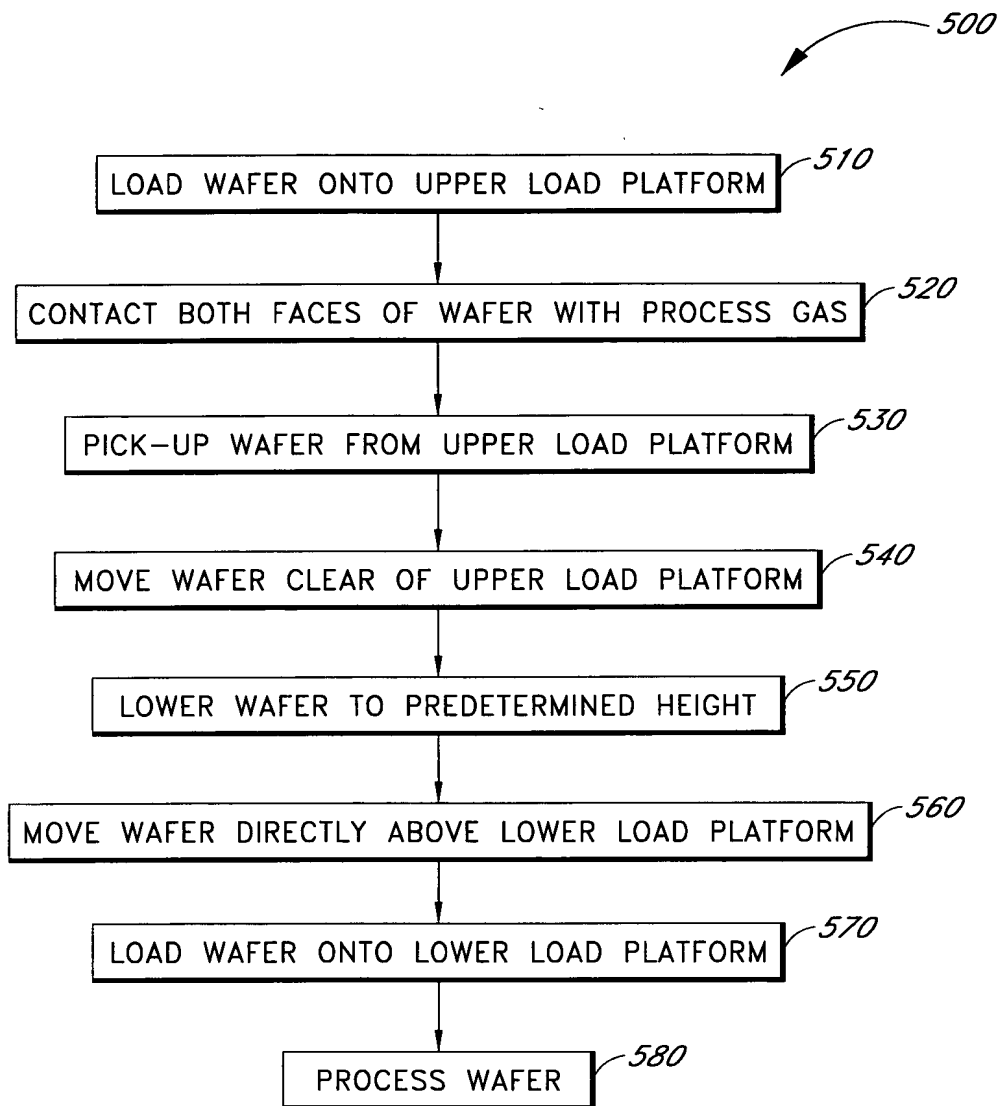
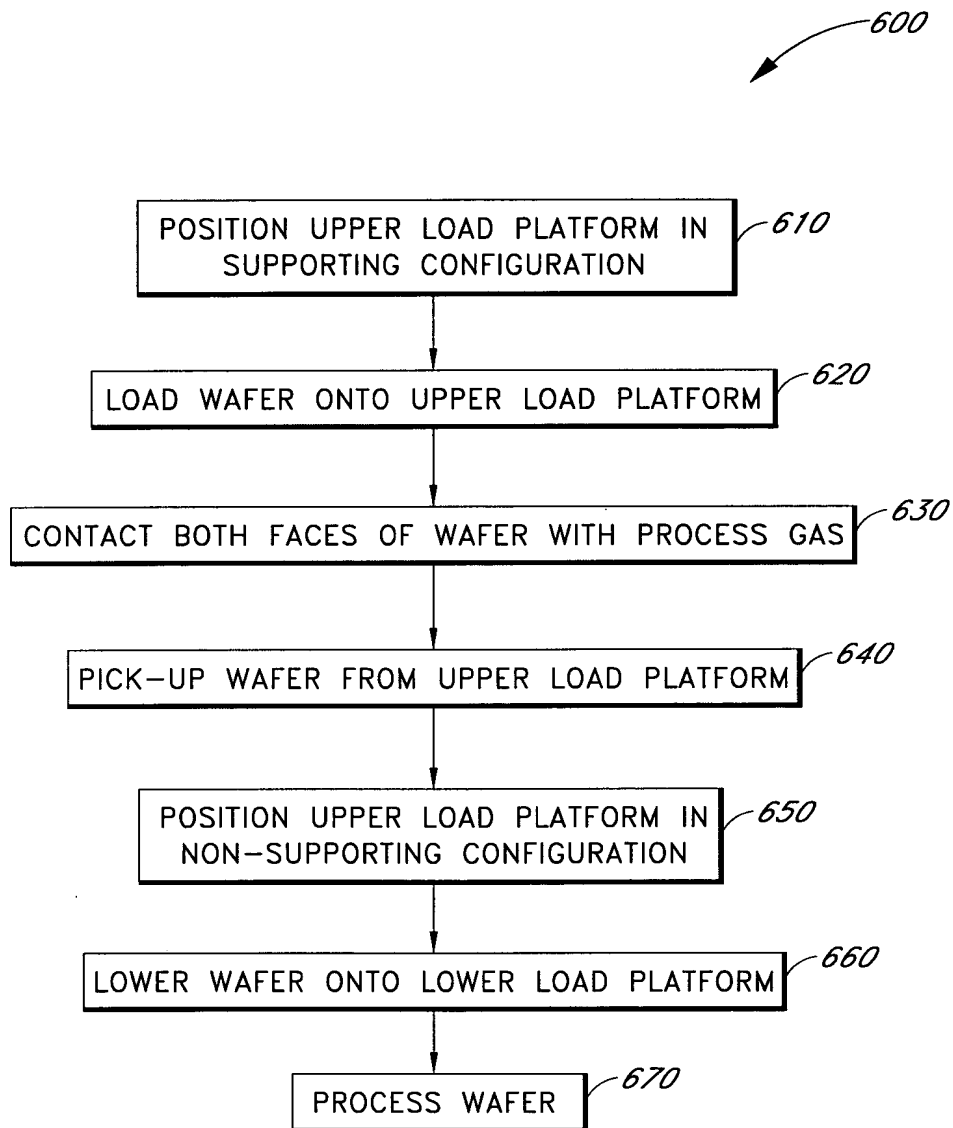


FIG. 5



*FIG. 6*